



U.S. **UTILITY** Patent Application
O.I.P.E. , PATER PATENT DATE

09/891324	CONT/PRIOR	CLASS 438- 250	SUBCLASS 3/0	ART UNIT	EXAMINER	
Osamu Nak	(agawa	438	2004	28/3	SCH, LIM	_ ~
Process f capacitor	or high- in VLSI	dielectr multi-l	ic constan evel metal	t metal-ins lization sy	ulator metal stems	

ISSUING CLASSIFICATION ORIGINAL **CROSS REFERENCE(S)** SUBCLASS SUBCLASS (ONE SUBCLASS PER BLOCK)

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TERMINAL DISCLAIMER	DRAWINGS			CLAIN	CLAIMS ALLOWED		
DISCEMINEN	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.		
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The term of this patent shall					•		
not extend beyond the expiration date of U.S Patent. No. **				ISSUE FEE			
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